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(57) Abstract :
Field programmable gate arrays (FPGA) are emerged in many digital signal processing (DSP) applications with the inclusion of dedicated core processing elements as logical blocks. But the technology remains limited in its ability to support high speed demands which gives rise unified arithmetic models to perform some core functional units. This paper presents high performance RNS arithmetic for Q-R decomposition (QRD) to perform matrix inverse core which is limiting the overall system performance of FPGA implementation of OMP algorithm for compressive sensing signal reconstruction. In this letter, we also introduce a new memory efficient on chip ram based reverse conversion unit that is useful for high speed RNS computation. This hardware optimized RNS architecture can takes wide range of input operand sizes with different sets of moduli sets. The design is implemented in on ALTERA FPGA Cyclone-II devices. Experimental results proved that this memory efficient reverse conversion RNS architecture outperform all other state-of-the-art FPGA implementation.

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